REMARKS

After entry of this amendment, claims 1, 3-13, and 15-29 are pending. In the present Office Action, claims 1-11, 13-21, and 23-29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Tran, U.S. Patent No. 6,016,533 ("Tran"). Claims 12 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran in view of Wickeraad et al., U.S. Patent No. 6,490,654 ("Wickeraad"). Applicants respectfully traverse these rejections and request reconsideration.

Applicants respectfully submit that claims 1, 3-13, and 15-29 recite combinations of features not taught or suggested in the cited art. For example, claim 1 recites a combination of features including: "the memory is configured to output a plurality of values from the set in response to the decoder selecting the set, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory, wherein the cache includes a same number of ways as the memory, and wherein the cache includes a tag memory storing a plurality of tags corresponding to cache lines stored in the cache and a data memory storing the cache lines …the circuit is configured to compare the first value to the plurality of values, and wherein a match of the first value and a second value stored in a first way of the plurality of ways causes the circuit to predict the first way to be a hit in the cache for the first address for the current access, and wherein the circuit is configured to output a way identifier identifying the first way to the data memory, the way identifier used by the data memory to select the first way to output data, and wherein the circuit is configured to construct the way identifier based on the comparisons of the first value to the plurality of values."

Applicants respectfully submit that Tran does not anticipate the above highlighted features. As noted in the most recent previous Response to Office Action (the "previous response," herein), Tran teaches way prediction for a data cache in which a plurality of storage locations store way predictions [Tran, col. 3, lines 20-22], and way predictions are selected from the storage locations based on a first portion of the input address [Tran, col. 3, lines 22-24]. The decoder selects a subset of the memory locations in the cache based on decoding a second portion of the address and the way predictions [Tran, col. 3,

lines 25-29]. It is important to note that these memory locations that are selected based on the way predictions and decoding the second portion of the address are not the locations storing the way predictions, but rather are the memory locations that store the cache lines themselves. In one embodiment, Tran's decoder selects a subset of the way predictions that were selected based on the first portion of the input address using the second portion of the input address [Tran, col. 3, lines 41-44].

Thus, to summarize, Tran selects way predictions based on a portion of an input address, and uses those way predictions and another portion of the input address to select a cache memory location from which to output data. Nowhere does Tran teach or suggest **predicting a first way to be hit** in the cache for the first address **responsive to the first value matching one of a plurality of values**, wherein the one of the plurality of values is **output from the first way of the memory** as recited in claim 1.

The Office Action responds to the above argument (see Office Action, page 2, paragraph number 4 that extends to page 3), asserting that Tran teaches predicting a first way responsive to the first value matching one of the plurality of values output from the first way. Specifically, the Office Action asserts that "for a way to be in the way prediction array, it must have been correct previously, so that specific way was compared in step 122 and either updated in step 124 or kept in step 126. Therefore, the outputting of a way from the way prediction array can be considered in response to it being added or kept in the way prediction array." Applicants respectfully disagree.

First, Applicants note that Tran does not compare a predicted way to a plurality of ways to determine that the predicted way was correct. Instead, Tran compares the predicted way to the single way that is actually hit: "If there is a hit in the tags, the way prediction is checked with the actual way (block 122)." (Tran, col. 15, lines 32-35). Thus, comparing the predicted way to the single hitting way cannot teach or suggest the first value matching one of the plurality of values, as recited in claim 1. The actual way is determined by comparing the input address to the tags (Tran, col. 15, lines 28-31). However, the tags cannot be the plurality of values recited in claim 1. Claim 1 explicitly

recites the tags separate from the plurality of values, and thus it is clear that the plurality of values are not the tags.

Furthermore, claim 1 recites that the circuit is configured to compare the first value to the plurality of values, and wherein a match of the first value and a second value stored in a first way of the plurality of ways causes the circuit to predict the first way to be a hit in the cache for the first address for the current access, and wherein the circuit is configured to output a way identifier identifying the first way to the data memory, the way identifier used by the data memory to select the first way to output data, and wherein the circuit is configured to construct the way identifier based on the comparisons of the first value to the plurality of values." Tran does not construct a way identifier based on the comparisons of the first value to the plurality of values.

Applicants noted that claim 1 explicitly recites the tags separately in the previous Response. The Office Action responds in paragraph 5 (page 3), stating that Applicants were contending that Tran does not teach a tags memory separate from the memory storing the values. That was not Applicants' intent. Applicants clarified claim 1 to ensure that the tag comparisons, performed by Tran to detect the hitting way as discussed above, were not interpreted as being the plurality of values that are matched to the first value to predict the first way. By reciting the plurality of tags separately, and thus clarifying that the plurality of values are not tags, claim 1 as clarified is clearly not anticipated by Tran.

The Office Action's analysis (in paragraph 4 of the Office Action) also fails to appreciate claim 1 as a whole. Claim 1 recites that the memory is configured to output a plurality of values from the set in response to the decoder selecting the set, and that the circuit is coupled to receive the plurality of values output from the memory. The circuit compares the plurality of values to a first value corresponding to the first address, and constructs a way identifier that identifies a first way in which a match is detected. The way identifier is transmitted to the data memory of the cache. Thus, Tran's discussion of determining the correct way that hits and storing that way as the way prediction to be

used at a later time does not teach or suggest receiving the plurality of values (output from the memory in response to the indication of the address that is to access the cache) and matching the plurality of values to a value corresponding to that address to predict the first way.

Viewed in another way, Tran stores way predictions and outputs them to select a cache memory location to output cache data. The stored values are the way predictions. Claim 1 recites storing values in a memory, outputting those values in response to an indication of the first address, and predicting the first way responsive to matching the first value to the plurality of values. Each way prediction in Tran, by contrast, corresponds to a set of cache lines and predicts which way in the set will hit.

Additionally, Applicants submit that Tran's way prediction array does not anticipate the recited memory having a plurality of ways that are the same in number as the plurality of ways in the cache. With respect to Fig. 3 of Tran, there appears to be no discussion of the structure of the way prediction array. In Fig. 4, the way prediction array 64 has an unusual structure that is clearly not the same number of ways as the cache.

For at least the above stated reasons, Applicants submit that claim 1 is patentable over the cited art. Claims 3-12 depend from claim 1 and recite additional combinations of features not taught or suggested in the cited art. Claims 13 and 23 recite combinations of features including features similar to those highlighted above. Accordingly, claims 13 and 23 are also patentable over the cited art. Claims 15-22 depend from claim 13 and recite additional combinations of features not taught or suggested in the cited art. Claims 24-29 depend from claim 23 and recite additional combinations of features not taught or suggested in the cited art.

Statement of Substance of Interview

On March 9, 2009, the undersigned and Examiner Dillon had a telephonic interview. Claim amendments similar in nature to those made in this Response were discussed. The prior art was also discussed, including Tran. Arguments similar to those

presented above were discussed, highlighting reasons why the amended claims are patentable over the cited art.

CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-97500/LJM.

Respectfully submitted,

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